REMARKS

Reconsideration and allowance is respectfully requested. Before entry of this amendment, claims 1-21 were pending. In the Office Action, claims 1-21 were rejected. In the present amendment, claims 1, 4, 11 and 16-18 are amended, and claims 22-23 are added. After entry of the amendment, claims 1-23 are pending.

I. Claim 19

Claim 19 is rejected under 35 U.S.C. § 102(b) as being anticipated by Bongiorno et al. (USP 6,292,045) (Office Action, p. 2, lines 12-13). Claim 19 recites, "(a) a processor having a system clock input lead . . . and (d) means for detecting whether the first clock signal is inadequate . . . wherein the means decouples the terminal from the system clock input lead and couples the second clock circuit to the system clock input lead without receiving any signal from the processor" (emphasis added). Bongiorno does not form the basis for a valid rejection under § 102(b) because Bongiorno does not disclose all of the limitations of claim 19. Specifically, Bongiorno does not disclose both a processor and a means, wherein the means decouples without receiving any signal from the processor.

With regard to claim 19, the Examiner states that Bongiorno discloses "(a) a processor (80) having a system clock input lead (column 4, lines 2-8) . . . and (d) means for detecting (timer 70) . . . wherein the means decouples (deselects) the terminal from the system clock input lead . . . without receiving any signal from the processor (Bongiorno discloses a clock selection circuit wherein a timer [70] that can be a separate circuit from the microprocessor [80] and detects a first clock circuit [10] . . . column 4, lines 9-34 and column 4, line 61 thru column 5, line 7)" (Office Action, p. 2, line 15 – p. 3, line 8) (emphasis added). Applicants respectfully disagree. Bongiorno does not disclose any embodiment that includes both timer 70 and microprocessor 80. In addition, Bongiorno does not

disclose that a system clock input lead of a processor is decoupled and coupled without receiving a signal from a processor.

Bongiorno discloses one embodiment with timer 70 (Figure 1A, col. 4, lines 9-38) and another embodiment with microprocessor 80 (Figure 1B, col. 5, lines 8-28). The embodiment of figure 1B of Bongiorno does not include timer 70 and therefore cannot be the basis for the Examiner's rejection, the Examiner having stated that timer 70 discloses the means for detecting.

The embodiment of figure 1A that includes timer 70 does not include microprocessor 80. The description of the embodiment of figure 1A from column 4, line 9, through column 5, line 7, does not mention microprocessor 80. With regard to the embodiment of figure 1A, Bongiorno does not disclose a system clock input lead of a microprocessor. Consequently, Bongiorno does not disclose that timer 70 decouples or couples any clock source from or to a system clock input lead of a microprocessor. Moreover, Bongiorno does not disclose that timer 70 "deselects" or "selects" any clock source, as the Examiner suggests. Bongiorno does not disclose that the switching means 66 of Bongiorno receives any select input signal from timer 70. The only output from timer 70 is a reset signal that is not received by controller 40, but rather is sent to a microprocessor that is not microprocessor 80. Bongiorno explains:

> "Finally, the controller 40 provides the selected clock signal to a counter or timer 70. It should be noted that the inventive circuit 100 maybe modified so as to provide the selected clock signal to any device that requires a clock signal in order to operate. Such a device may be a microprocessor 80 as shown in FIG. 1B, a digital signal processor, an application-specific integrated circuit, a reduced instruction set computer, or a microcontroller.
>
> Referring again to FIG. 1A, the timer 70 may be a component of a microprocessor-based chip or an integrated circuit that also contains a microprocessor. If so, the timer 70 is preferably a watchdog timer that generates a signal to reset the microprocessor and disable the integrated circuit when the integrated circuit experiences a control failure or a lockup." (Bongiorno, col. 4, lines 1-15) (emphasis added)

Thus, Bongiorno does disclose that timer 70 sends a reset signal to a

microprocessor when a clock source malfunctions but does not disclose that any clock source is selected by controller 40 without receiving a signal from the microprocessor.

With regard to the embodiment of figure 1B that does not include timer 70, Bongiorno discloses that microprocessor 80 selects the clock source. Thus, Bongiorno also does not disclose that the embodiment of figure 1B selects a clock source without receiving a signal from microprocessor 80. To the contrary, microprocessor 80 selects the clock source "via the inventive circuit 100". Bongiorno states:

> "As a design choice, the controller 40 may be modified so as to output a warning signal to alert a microprocessor of a microprocessor-based system that the accurate clock source is no longer available. Based on a particular application, it may be desirable to pre-program the microprocessor 80 either to [1] shut down the microprocessor-based system or [2] select another clock source via the inventive circuit 100 when the microprocessor 80 receives the warning signal." (Bongiorno, col. 5, lines 21-28) (emphasis added)

Therefore, Bongiorno does not disclose any embodiment with both a processor and a means, wherein the means decouples a clock signal terminal from the system clock input lead of the processor without receiving any signal from the processor. Because Bongiorno does not disclose all of the elements of claim 19, reconsideration of the § 102(b) rejection and allowance of claim 19 are requested.

II. Claims 1-18

Claims 1-18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Bongiorno in view of Kim et al. (USP 6,845,454) (Office Action, p. 3, lines 17-19). To establish a *prima facie* case of obviousness, the Examiner must demonstrate three criteria. The MPEP § 2142 states:

> "To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or

> motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the reference (or references when combined) must teach or suggest all the claimed limitations." MPEP § 2142 (emphasis added).

A. Independent claim 1

The combination of Bongiorno and Kim does not form the basis for a valid rejection of claim 1 under § 103(a) because, among other things, the references when combined do not teach or suggest all of the claim elements. Claim 1 as amended recites "decoupling the first clock circuit from a system clock input lead of a processor, wherein the decoupling is not performed as a result of a signal from the processor". Neither Bongiorno nor Kim teaches decoupling a clock circuit from a system clock input lead of a processor that is not performed as a result of a signal from the processor.

The Examiner states that Bongiorno teaches "decoupling the first clock circuit in (b) is not performed as a result of a signal from the processor (Bongiorno discloses the decoupling [deselecting] is carried out as a result from the watchdog timer [70] which may or may not be part of the microprocessor; column 4, lines 9-21)" (Office Action, p. 6, lines 3-6) (emphasis added). Applicants respectfully disagree. Bongiorno does not teach that deselecting is carried out as a result of the watchdog timer 70 but not as a result of a signal from a microprocessor. Kim also does not teach the decoupling of a clock circuit that is not performed as a result of a signal from a processor.

First, Bongiorno does not teach that timer 70 is part of "the microprocessor", as the Examiner states. Instead, Bongiorno teaches that "the timer 70 may be a component of a microprocessor-based chip or an integrated circuit that also contains a microprocessor. If so, the timer 70 is preferably a watchdog timer that generates a signal to reset the microprocessor . . ."

(Bongiorno, col. 4, lines 9-13). Instead of being part of the microprocessor, as the Examiner states, the timer 70 sends a reset signal to the microprocessor.

Moreover, Bongiorno does not teach that timer 70 decouples or couples any clock source from or to a system clock input lead of a microprocessor. The embodiment of figure 1A that includes timer 70 does not include microprocessor 80. With regard to the embodiment of figure 1A, Bongiorno does not teach a system clock input lead of a microprocessor. Consequently, Bongiorno does not teach that timer 70 decouples or couples any clock source from or to a system clock input lead of a microprocessor. Moreover, Bongiorno does not teach that timer 70 "deselects" or "selects" any clock source, as the Examiner suggests. Bongiorno does not teach that the switching means 66 of Bongiorno receives any select input signal from timer 70. The only disclosed output from timer 70 is a reset signal that is not received by controller 40, but rather is sent to a microprocessor that is not microprocessor 80. Instead of teaching that a clock source is selected by controller 40 without receiving a signal from the microprocessor, Bongiorno teaches that timer 70 sends a reset signal to a microprocessor when a clock source malfunctions.

With regard to the embodiment of figure 1B that does not include timer 70, Bongiorno discloses that microprocessor 80 selects the clock source. Thus, Bongiorno also does not disclose that the embodiment of figure 1B selects a clock source without receiving a signal from microprocessor 80.

In addition, the clock generation circuit of Kim does not change a processor clock without receiving an external instruction. Kim does not teach that the external instruction that is decoded by instruction decoder 150 is not received from the processor. In fact, the Examiner admits that the clock selection circuit of Kim receives a "sleep" command from the processor. The Examiner states, "Kim teaches the detection circuit of the clock selection circuit receives a "sleep" command from the processor itself which is the device detecting the sent interrupts and sleep commands to the unwanted fast clock off; column 3, lines 26-34" (Office Action, p. 6, lines 17-20) (emphasis added).

Finally, there is no motivation to combine the teachings of Kim with the teachings of Bongiorno. Bongiorno is directed to a safety means that secures a clock signal in order to operate when a clock source malfunctions and no longer generates any clock signal. (Bongiorno, col. 4, lines 17-21). Kim is directed to using power-down and power-up instructions to change the operation mode of a processor built in a CDMA chip. (Kim, col. 5, lines 19-41) One of ordinary skill in the art would not have been motivated to modify the method of switching malfunctioning clocks of Bongiorno by including the power-down and power-up instructions of Kim because a processor that is receiving a malfunctioning clock cannot generate the instructions of Kim that switch to a power-saving clock.

Because the combination of Bongiorno and Kim does not disclose all of the elements of claim 1 and because there is no motivation to modify Bongiorno with the teachings of Kim, Bongiorno and Kim do not form the basis for a valid rejection under § 103(a). Reconsideration of the § 103(a) rejection and allowance of claim 12 are requested.

B. Dependent claims 2-10

Claim 2 recites that the first clock circuit is a high-speed, external crystal oscillator, that the second clock circuit is a low-speed, internal watchdog timer, and that the third clock circuit is a high-speed, internal oscillator. The Examiner states that "Bongiorno discloses a clock circuit having the ability to comprise various types of both internal and external clock sources that can be any combination of such [clocks]" (Office Action, p. 5, lines 13-14) (emphasis added). Applicants respectfully traverse this rejection. Bongiorno does not teach that the clock sources 10, 20 and 30 "can be any combination" of the possible clock types mentioned in the background section of Bongiorno. In fact, Bongiorno suggests the contrary:

> "It should also be noted that if only one of the clock sources 10, 20 and 30 is capable of providing accurate electrical signal frequencies and the programmed code designates such clock source as a first

> choice, it may not be desirable to employ the inventive circuit 100 in applications where the accuracy of the clock source is critical. The obvious reason is that the automatic selection of one of the undesignated and inaccurate clock sources when the designated clock source is not available, is undesirable." (Bongiorno, col. 5, lines 12-20) (emphasis added)

Claim 8 recites "disabling a failure detection circuit". The Examiner states that Kim teaches disabling a failure detection circuit. (Office Action, p. 6, lines 16-17) Kim does not, however, even mention a failure detection circuit. Kim does not teach that the first clock generator 110 or the second clock generator 120 ever fails, and consequently does not teach that such a failure can be detected. A processor detecting interrupt commands, which the Examiner points to, does not teach a failure detection circuit detecting whether a clock signal is inadequate. Because Kim does not teach a failure detection circuit, Kim also does not teach disabling a failure detection circuit.

Claim 10 recites, "wherein a third data input lead of the multiplexer is grounded, and wherein between step (b) and step (c) the multiplexer couples the third data input lead of the multiplexer to the system clock input lead" (emphasis added). Although the Examiner restates the terms of claim 10, the Examiner does not make a *prima facie* argument of obviousness. The Examiner states that the combination of Bongiorno and Kim "can provide a three-input multiplexer to select any of the three desired clock signals". (Office Action, p. 7, lines 11-12). The Examiner does not argue, however, that either Bongiorno or Kim teaches coupling a system clock input lead to ground. Figure 4 of Kim shows that the processor clock signal P_CLOCK is either CLOCK 1 or CLOCK 2, but is never grounded.

In addition to the reasons states above, claims 2-10 depend directly or indirectly from claim 1 and are allowable for at least the same reasons for which claim 1 is allowable. Reconsideration of the § 103(a) rejection and allowance of claims 2-10 are requested.

C. Independent claim 11

The combination of Bongiorno and Krulce does not form the basis for a valid rejection of claim 11 under § 103(a) because, among other things, the references when combined do not teach or suggest all of the claim elements. Claim 11 as amended recites "the clock controller is adapted to . . . couple the system clock input lead to the second clock circuit upon detecting that the first clock signal has failed, and wherein the clock controller is further adapted to turn on the third clock circuit upon detecting that the first clock signal has failed". (emphasis added). Neither Bongiorno nor Kim teaches turning on a clock circuit upon detecting that another clock circuit has failed.

The Examiner admits that Bongiorno fails to disclose a clock controller adapted to turn on a third clock circuit. (Office Action, p. 8, lines 9-10) In addition, neither Bongiorno nor Kim teaches a clock controller adapted to turn on a third clock circuit upon detecting that a first clock signal has failed. Kim does not teach a clock controller adapted to turn on a clock circuit upon detecting that another clock signal has failed. The clock generation circuit 10 is not adapted to detect that a clock signal has failed.

The Examiner fails to present a *prima facie* argument of obviousness because the Examiner does not even state that either Bongiorno or Kim teaches a clock controller adapted to turn on a clock circuit upon detecting that another clock signal has failed. Instead, the Examiner states, "It would have been obvious . . . to modify the clock switching method of Bongiorno to include the ability to power off unnecessary clock circuits as taught by Kim such that when selecting a clock to use the clock circuit is enabled/powered on first then coupled and the failing/unnecessary clock is disabled/powered off" (Office Action, p. 8, lines 17-21) (emphasis added). Teaching the powering off of unnecessary clock circuits while all clock circuits are functioning does not teach turning on a clock circuit upon detecting that another clock signal has failed.

The teachings of Kim do not teach enabling a clock circuit upon detecting that the clock signal, which is coupled to the system clock input lead of the

processor, has failed. The Examiner admits that the clock selection circuit of Kim receives commands from the processor by stating, "Kim teaches the detection circuit of the clock selection circuit receives a "sleep" command from the processor itself which is the device detecting the sent interrupts and sleep commands to the unwanted fast clock off; column 3, lines 26-34" (Office Action, p. 6, lines 17-20) (emphasis added). Kim does not teach enabling a clock circuit upon detecting that the clock signal that is coupled to the system clock input lead of the processor has failed because the clock selection circuit of Kim relies on commands from the processor to enable a different clock generator.

For the same reason, there can be no motivation to combine the teachings of Kim with the clock controller 40 of Bongiorno because the clock selection circuit of Kim relies on commands from a processor to power up a new clock generator, and the processor would be clocked by a failed clock from the old clock generator. One of ordinary skill in the art would not have been motivated to modify the method of switching malfunctioning clocks of Bongiorno by including the power-up instructions of Kim because the processor that receives the malfunctioning clock cannot generate the instructions of Kim that switch to a functioning clock. Thus, there is no expectation of success in combining the teachings of Kim with the method of switching malfunctioning clocks of Bongiorno.

Because the combination of Bongiorno and Kim does not disclose all of the elements of claim 11 and because there is no motivation to modify Bongiorno with the teachings of Kim, Bongiorno and Kim do not form the basis for a valid rejection under § 103(a). Reconsideration of the § 103(a) rejection and allowance of claim 11 are requested.

D. Dependent claims 12-18

Claim 12 recites that the first clock circuit is a high-speed, external crystal oscillator. The Examiner states that "Bongiorno discloses a clock circuit having the ability to comprise various types of both internal and external clock sources

that can be any combination of such [clocks]" (Office Action, p. 9, lines 5-7). Applicants respectfully disagree. Bongiorno does not teach that the clock sources 10, 20 and 30 "can be any combination" of the possible clock types mentioned in the background section of Bongiorno. As explained with regard to claim 2, Bongiorno in fact suggests the contrary.

Claim 13 recites that the second clock circuit is a low-speed, internal watchdog timer oscillator. The Examiner states that "Bongiorno discloses the integrated circuit wherein the second clock circuit is a low-speed, internal watchdog timer (column 4, lines 9-15) . . ." (Office Action, p. 9, lines 10-11). Bongiorno, however, does not disclose that any of clock sources 10, 20 or 30 is a watchdog timer. The passage of Bongiorno cited by the Examiner states that timer 70, as opposed to any of the clock sources 10, 20 or 30, is a watchdog timer:

> ". . . the timer 70 is preferably a watchdog timer . . . the programmed code received by the controller 40 designates the clock source 10 as a first choice for providing the clock signal to the timer 70. Thus, clock sources 20 and 30 are essentially safety means from which the timer 70 secures a clock signal in order to operate when the clock source 10 becomes malfunctioned and no longer generates any clock signal" (Bongiorno, col. 4, lines 12-21) (emphasis added)

In addition to the reasons states above, claims 12-18 depend directly or indirectly from claim 11 and are allowable for at least the same reasons for which claim 11 is allowable. Reconsideration of the § 103(a) rejection and allowance of claims 12-18 are requested.

E. Dependent claims 20-21

Claims 20-21 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Bongiorno in view of Kim (Office Action, p. 10, lines 19-22). Claims 20-21 include the following limitations of base claim 19, "a processor having a system clock input lead . . . wherein the means decouples the terminal

from the system clock input lead . . . without receiving any signal from the processor". Bongiorno and Kim do not form the basis for a valid rejection of claims 20 and 21 under § 103(a) because neither Bongiorno nor Kim teaches a means that decouples a terminal from a system clock input lead without receiving any signal from a processor.

The Examiner admits that the clock selection circuit of Kim receives commands from the processor. The Examiner states, "Kim teaches the detection circuit of the clock selection circuit receives a "sleep" command from the processor itself which is the device detecting the sent interrupts and sleep commands to the unwanted fast clock off; column 3, lines 26-34" (Office Action, p. 6, lines 17-20) (emphasis added). Thus, Kim does not teach a means that decouples without receiving any signal from a processor.

Bongiorno also does not teach that a system clock input lead of a processor is decoupled without receiving a signal from the processor. The embodiment of figure 1A that includes timer 70 does not include microprocessor 80. With regard to the embodiment of figure 1A, Bongiorno does not teach a system clock input lead of a microprocessor. Consequently, Bongiorno does not teach that timer 70 decouples any clock source from a system clock input lead of a microprocessor. Moreover, Bongiorno does not teach that the switching means 66 receives any select input signal from timer 70 or that timer 70 "deselects" any clock source. The only output from timer 70 is a reset signal that is not received by controller 40, but rather is sent to a microprocessor that is not microprocessor 80.

With regard to the embodiment of figure 1B that does not include timer 70, Bongiorno discloses that microprocessor 80 selects the clock source. Thus, Bongiorno also does not disclose that the embodiment of figure 1B selects a clock source without receiving a signal from microprocessor 80. To the contrary, microprocessor 80 selects the clock source "via the inventive circuit 100". (See Bongiorno, col. 5, lines 21-28) Therefore, Bongiorno does not disclose any embodiment with both a processor and a means, wherein the means decouples

a clock signal terminal from the system clock input lead of the processor without receiving any signal from the processor.

Reconsideration of the § 103(a) rejection and allowance of claims 20-21 are requested.

III. New claims 22-23

Applicants are adding new depedent claims 22-23, each of which is supported by the specification and allowable over the cited reference. No new matter is added.

IV. Conclusion

In view of the foregoing amendments and remarks, Applicants respectfully submit that the entire application (claims 1-23 are pending) is in condition for allowance. Applicants respectfully request that a timely Notice of Allowance be issued in this case. If the Examiner would like to discuss any aspect of this application, the Examiner is requested to contact the undersigned at (925) 621-2121.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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